WinTechCon 2026 - Call for Papers

IMPORTANT DATES

Deadline for submission of Papers/Tutorials/Demos	: May 17, 2026
Communication of acceptance to Authors	: September 7, 2026
Conference	: November 18-19, 2026

THEME, OBJECTIVE & FOCUS

THEME

Empowering Innovation: From Intelligent Silicon to Global Ecosystems

OBJECTIVE

The objective is to provide opportunities for women leaders in technology to present their work in emerging technical fields, strengthening inclusive technical leadership and amplifying diverse voices driving innovation.

FOCUS AREA

The conference invites thought leaders, researchers, and industry pioneers to present contributions that demonstrate how novel device- and circuit-level innovations translate into robust, scalable systems; how AI and domain-specific hardware are architected, implemented, and deployed; how reliability, testability, and manufacturability are engineered into increasingly complex semiconductor designs; how advanced design methodologies and EDA tools enable faster turnaround for challenging problems; and how innovative approaches to verification, packaging, validation, and system integration contribute to resilient, high-performance technology ecosystems.

SUBMISSION TRACKS

Authors are invited to submit their original, unpublished research work through the Microsoft CMT tool: Conference Management Toolkit - Author Console under the following tracks for papers, demos and tutorials:

TRACKS

Track 1: Intelligent Silicon, VLSI Design, and Architecture

Track 2: AI Accelerators, Custom Hardware, and In/Near Memory Computing

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Track 3: Embedded Systems, Real Time Computing, and Automotive/Industrial Electronics

Track 4: Security, Reliability, and Trustworthy Semiconductor Systems

Track 5: Design-for-Test (DFT), Physical Design, Test yield and manufacturability

Track 6: Design Verification and Validation

Track 7: Semiconductor Packaging, Heterogeneous Integration, and System Level Design

Submission link:
https://cmt3.research.microsoft.com/WINTECHCON2026/Submission/Index

All the accepted and presented papers will be submitted to IEEE Xplore for possible publication, ensuring quality, global visibility and recognition.

TRACKS

Track 1: Intelligent Silicon, VLSI, Analog/Mixed-Signal, and Architecture

This track covers digital, analog, mixed-signal (AMS), and RF circuit design, along with advanced architectures for CPUs, GPUs, NPUs, heterogeneous SoCs, chiplets, and 2.5D/3D ICs. Topics include low-power and high-performance digital, analog, mixed-signal, and RF circuits, as well as emerging and unconventional computing paradigms. Contributions on CAD tools, physical design optimization, and architecture-level innovation are also welcome.

Track 2: AI Accelerators, Custom Hardware, and In-/Near-Memory Computing

This track invites papers on domain-specific and AI/ML accelerators, neuromorphic computing, in-memory and near-memory computing architectures, energy-efficient AI hardware, quantum-inspired and approximate computing, as well as co-design of algorithms, compilers, and runtime systems for specialized hardware.

Track 3: Embedded Systems, Real-Time Computing, and Automotive/Industrial Electronics

This track covers embedded platforms and real-time systems for automotive, industrial, robotics, and autonomous applications. Topics include hardware/software co-design, safety and certification (e.g., ISO 26262), dependable cyber-physical systems (CPS), and platform software for constrained and safety-critical environments.

Track 4: Security, Reliability, and Trustworthy Semiconductor Systems

Security is a critical challenge in semiconductor development. This track focuses on hardware and system security, secure SoCs and accelerators, reliability and fault tolerance for complex and 3D-integrated systems, in-field monitoring, and silicon lifecycle management.

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Track 5: Design-for-Test (DFT), Physical Design, Test Yield, and Manufacturability

This track invites innovations in design-for-test methodologies, test automation, and built-in self-test (BIST) techniques. Contributions are encouraged on yield enhancement strategies, defect modeling, adaptive test approaches, and manufacturability solutions that improve efficiency, scalability, and cost-effectiveness in semiconductor production. This track also includes innovations in physical design, place-and-route optimization, timing closure, power integrity, congestion management, signoff methodologies, and physical implementation techniques for advanced process nodes.

Track 6: Design Verification and Validation

This track invites contributions in formal and dynamic verification, emulation, and FPGA prototyping for functional and system validation. System methodologies and EDA tools supporting the silicon lifecycle are also welcome.

Track 7: Semiconductor Packaging, Heterogeneous Integration, and System-Level Design

This track focuses on advanced packaging technologies (2.5D/3D integration, chiplets, system-in-package), heterogeneous integration of logic, memory, RF, sensors, and power components, signal and power integrity, thermal management, co-design across silicon–package–board–system hierarchies, and sustainability and reliability aspects of integrated systems.

CATEGORY OF SUBMISSION

TECHNICAL PAPERS

All accepted and presented papers will be submitted to IEEE Xplore for possible publication, ensuring quality, global visibility, and recognition. In addition to papers presenting innovative and significant advancements in the current state of the art, submissions describing impactful product-engineering innovations are also welcome. These may include novel inventions, improvements in engineering processes, cross-pollination of ideas, surveys, design flows, methodologies, process enhancements, and practical knowledge applied to real-world product development across the aforementioned areas.

TUTORIALS

- Tutorial presenters are expected to be well recognized in the subject area and/or have several years of relevant work experience.
- Include the following materials:
    - Title and anonymous abstract (300 words) in a PDF
    - Biography of the presenters in a separate PDF
    - Anonymous tutorial slides in PPT format
- Tutorials may have no more than two presenters, with at least one woman presenter.
- The tutorial duration will be one hour.

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- The abstract and slides should clearly describe the importance of the proposed topic, the content to be covered, and the expected audience takeaway.
- The proposal must clearly articulate the motivation and organization of the tutorial.

PROJECT DEMOS

Include the following materials:

- Title and anonymous abstract (300 words) in a PDF
- Biography of the presenters in a separate PDF
- Anonymous project demo description in a PDF

The project demo description must include the background and objectives of the project, the problem being addressed, the methodology and implementation steps, the format and expected results of the demonstration, and the audience takeaway.

Demos may have no more than two presenters, with at least one woman presenter.

SUBMISSION GUIDELINES

- All submissions must be anonymous and strictly between 4 and 6 pages.
- The standard IEEE double-column conference format must be followed.
- Do not identify the author(s) by name or affiliation anywhere in the manuscript or abstract.
- References to the authors' own prior work or affiliations must be written in the third person in the bibliography and throughout the manuscript.
- Avoid the use of "omitted for blind review" in the bibliography.
- Orphan references (i.e., references not cited in the manuscript) must not appear in the bibliography.
- A minimum of six references must be included and cited within the manuscript.
- At least four references must be external to the submitter's organization.

Papers will be reviewed under the condition that they contain no plagiarized material and have not been submitted to another conference or publication venue concurrently (double submission). Violations of these policies will be handled in accordance with IEEE guidelines.

Authors are encouraged to review IEEE's policies on plagiarism and multiple submissions at: https://conferences.ieeeauthorcenter.ieee.org/author-ethics/guidelines-and-policies/submission-policies/

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FORMAT OF TECHNICAL PAPER SUBMISSION

- Each paper must be limited to six A4 pages in IEEE double-column format using 10-point font, including figures and tables.
- Authors must follow the IEEE Conference Format template, available at: https://www.ieee.org/conferences/publishing/templates.html
- Papers may have no more than six authors and two presenters, with at least one woman author and one woman presenter. The primary author should be a woman.
- The submission must include the full paper in PDF format, prepared in compliance with the anonymous review guidelines.

POINTS TO REMEMBER

- The primary author/presenter of the paper **SHOULD BE a FEMALE**. Co-authors/co-presenters can be a MALE or FEMALE.
- All submission manuscripts and abstracts **MUST BE** anonymous without revealing author names and affiliations.
- Professionals from the technology industry (semiconductor/hardware/software) and academia may submit.
- IEEE format **SHALL BE** followed. Failing it will result in rejection
- All the co-authors **MUST BE** shown in the initial submission. No further authors can be added for selected papers.
- Technical paper submissions can be accepted either for paper presentation or poster presentation, based on discretion of the TPC. The final PPT should be formatted accordingly, based on the acceptance notification.
- If a manuscript is accepted for paper presentation, the authors will be expected to submit a final version of the manuscript that will be added to IEEE proceedings

ANONYMOUS SUBMISSIONS

- To comply with IEEE review requirements, all submission manuscripts **MUST BE anonymous.**
- **DO NOT** identify the author(s) by their name(s) or affiliation(s) anywhere on the manuscript or abstract.
- All references to the author(s) own previous work or affiliations in the Bibliographic citations must be in the third person.
- **AVOID** the use of “omitted for blind review” in the Bibliography section

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ACKNOWLEDGEMENT

The Microsoft CMT service was used for managing the peer-reviewing process for this conference. This service was provided for free by Microsoft and they bore all expenses, including costs for Azure cloud services as well as for software development and support.

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