

IEEE WINTECHCON 2022

Technical Conference by Women in Engineering

June 2 & 3, 2022 | Venue: Virtual

Theme: Smarter technologies for a sustainable and hyper-connected world

Platinum Patron
& Host
Qualcomm

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ANALOG DEVICES IBM infineon SAMSUNG

AGENDA

DAY 1	Venue	Time	Particulars
	Audi 1	09:00 - 09:30 AM	Welcome Note
	Audi 1	09:30 - 10:30 AM	Grand Summit Keynote by Karen Bartleson with Q & A
	Booths/ Networking Zone	10:30 - 11:00 AM	Visit Sponsor Booths / Break / Poster, Project Demo, PhD Forum Booths
	Track 1	11:00 - 11:40 AM	Tutorial: AI/ML & Big Data Emerging Techniques of Information-Retrieval from Text and Tabular data in Advanced Q&A Systems - Sakina Pitalwala (Intel); Ruma Mukherjee (Intel)
	Track 1	11:40 - 12:00 PM	Algorithms and Applications of AI, ML & Big Data Refinement Of Reinforcement Learning Algorithms Guided By Counterexamples - Bittu Gangopadhyay (Indian Institute of Technology Kharagpur); Somi Vishnoi (IIT Kharagpur); Pallab Dasgupta (IIT Kharagpur)
	Track 1	12:00 - 12:20 PM	Enabling Smart Building Applications on the Edge using Artificial Intelligence - Raka Singh (Analog Devices)
	Track 1	12:20 - 12:40 PM	SiBo-The Sign Bot, Connected world for disabled - Nihitha Rajasekhar (Infineon Technologies India Pvt. Ltd.); Swarnam Panday (Infineon Technologies)
	Track 1	12:40 - 01:00 PM	A Faster Approach For Direct Speech to Speech Translation - Rashmi T S (Samsung R&D Institute India-Bangalore); Sourabh Tewari (Samsung R&D Institute India-Bangalore)
	Track 2	11:00 - 11:40 AM	Tutorial: VLSI & EDA Ride High: Achieve success in complex low power SoC design using smart UPF Strategies - Kritika Rampal (Intel); dhanopathy krishnamoorthy (Intel India); sreehari karnam (Intel India)
	Track 2	11:40 - 12:00 PM	Pre-silicon Verification Formal Verification of Deep Neural Networks in Hardware - Shreyansh Agrawal (Intel Tech India Pvt Ltd); Surinder Sood (Intel Technology India Pvt Ltd); Sincy Ann Sajj (Intel Technology India Pvt Ltd)
	Track 2	12:00 - 12:20 PM	A Holistic Approach to CPU Verification using Formal Techniques - Bhavya Sri Dasari (Texas Instruments); Karthik Rajakumar (Texas Instruments); Pooja M (Texas Instruments); Venkata Nitin Edaropalli (Texas Instruments)
	Track 2	12:20 - 12:40 PM	Deploying SEC for Design Cycle Time Reduction and Quality Improvement - Varshashree Kottadamane (Texas Instruments); Naveen Kothuri (Texas Instruments); Saravanan Gajendran (Texas Instruments); Dewi A (Texas Instruments); Narendra Ravilla (Texas Instruments); Labeeb K (Texas Instruments); Sai Langadi (Texas Instruments)
	Track 2	12:40 - 01:00 PM	A hardware-software approach for model downloading in multi-fpga platforms - Vani V (Intel); Mark Hicid (Intel); Gary McGee (Intel); Balaji G (Intel); Vikas Akalwadi (Intel)

DAY 2	Venue	Time	Particulars
	Audi 1	09:00 - 09:30 AM	Welcome Note
	Audi 1	09:30 - 10:30 AM	Grand Summit Keynote by Vanitha Kumar with Q & A
	Booths/ Networking Zone	10:30 - 11:00 AM	Visit Sponsor Booths / Break / Poster, Project Demo, PhD Forum Booths
	Track 1	11:00 - 11:40 AM	Tutorial: Emerging Technologies/Open-Source Technology Demystifying Device Tree Concepts - Priya Dixit (Samsung Semiconductor Research India)
	Track 1	11:40 - 12:00 PM	Cloud, Compute, Security, Mobile Communications, Connectivity Simplified near Data Placement Processing Layout for Distributed Storage Object Systems - Subhashini Mohan (HCL); Ian Adams (Intel); Santhoshkumar Nallamolla (HCL); Aaditya Sharma (HCL)
	Track 1	12:00 - 12:20 PM	Adaptive DRX mechanism to improve Energy Efficiency and to reduce Page Delay for VoWifi Devices - Deepthi Bala Dash (Samsung Semiconductor India R&D, Bangalore); Goutham Pannamreddy (Samsung); Umasonkar Ceandhraku Baskar (Samsung Semiconductor India R&D, Bangalore); Prasad Basavaraj Dandra (Samsung Semiconductors Bangalore)
	Track 1	12:20 - 12:40 PM	AI layer reference generator engine for early enablement of workloads over multiple frameworks - Mansi Agarwal (Intel); Swadesh Verma (Intel); Pramod Kumar (Intel); Chandan Kumar (Intel)
	Track 2	11:00 - 11:40 AM	Tutorial: Internet of Things - Wearables Wearable Devices and Body Area Networks - Salma Fauzia (Muffakham Jah College of Engineering and Technology)
	Track 2	11:40 - 12:00 PM	Data and ML Solutions for EDA Relevancy of Replacing NFS with Storage Buckets in EDA Industry - Harisree LNU (Synopsys); Lokesh Babu Rao (Synopsys); Sai Nikhil Guntur (Synopsys); Radha Srinivasan (Synopsys)
	Track 2	12:00 - 12:20 PM	Challenges in Building Deployable Machine Learning Solutions for SoC Design - Shilpi Kapoor (Qualcomm); Payal Agarwal (Qualcomm); Lindsey Kostas (Qualcomm Technologies, Inc.)
	Track 2	12:20 - 12:40 PM	High Performance Field Configurable Data Re-alignment Engine - Yaswani Priyanka Vempalli (Samsung Semiconductor India Research); Shriharsha Kolla (Samsung Semiconductor India Research); Kiran Lumar Muraldharan (Samsung Semiconductor India Research); Vulligadla Amanesh (Samsung Semiconductor India Research)
	Track 2	12:40 - 01:00 PM	High Speed IO Access for Test - Kranthi Kandula (Synopsys); Armit Kapatkar (Synopsys); Hamasagar Babur Reddy (Synopsys)
	Audi	01:00 - 01:30 PM	Awards Ceremony